

# DATA SHEET

## **74LVT16240A**

**3.3V LVT 16-bit inverting buffer/driver  
(3-State)**

Product specification  
Supersedes data of 1994 Dec 15  
IC23 Data Handbook

1998 Feb 19

# 3.3V 16-bit inverting buffer/driver (3-State)

# 74LVT16240A

## FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

## DESCRIPTION

The 74LVT16240A is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3V.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ( $1\overline{OE}$ ,  $2\overline{OE}$ ,  $3\overline{OE}$ ,  $4\overline{OE}$ ), each controlling four of the 3-State outputs.

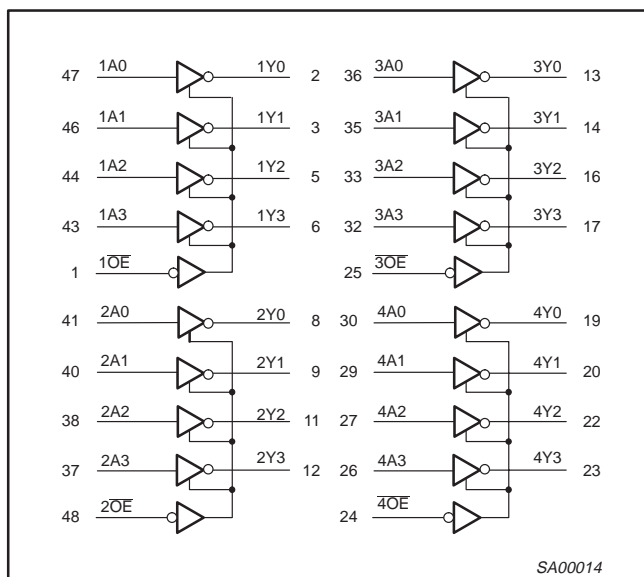
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay $nAx$ to $n\overline{Y}x$	$C_L = 50pF$ ; $V_{CC} = 3.3V$	1.9	ns
$C_{IN}$	Input capacitance $n\overline{OE}$	$V_i = 0V$ or $3.0V$	3	pF
$C_{OUT}$	Output capacitance	Outputs disabled; $V_O = 0V$ or $3.0V$	9	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 3.6V$	70	$\mu A$

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to +85°C	74LVT16240A DL	VT16240A DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74LVT16240A DGG	VT16240A DGG	SOT362-1

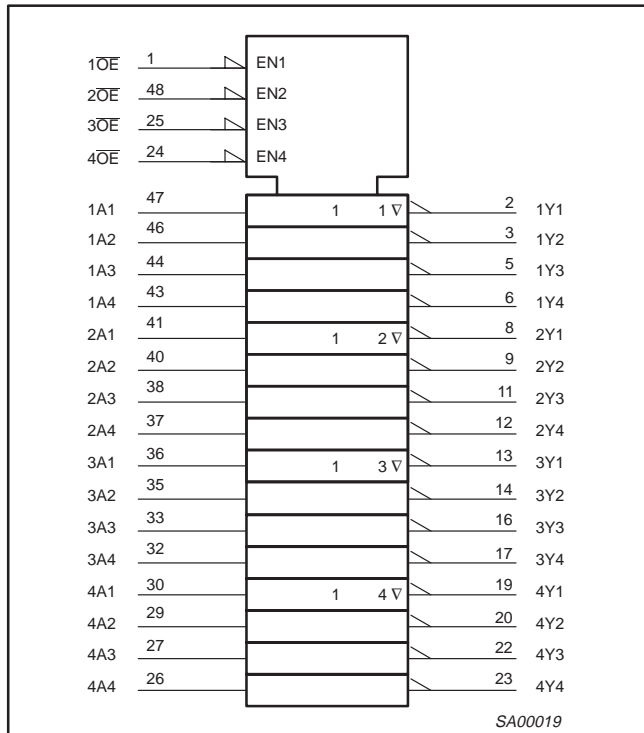
## LOGIC SYMBOL



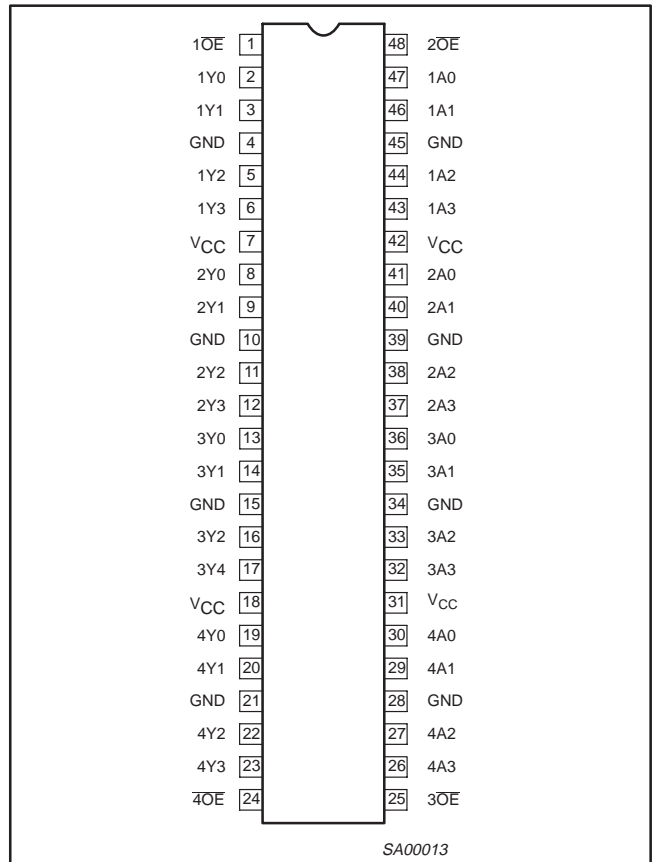
# 3.3V 16-bit inverting buffer/driver (3-State)

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## LOGIC SYMBOL (IEEE/IEC)



## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Y0-1Y3 2Y0-2Y3 3Y0-3Y3 4Y0-4Y3	Data outputs
1, 48, 25, 24	1OE, 2OE, 3OE, 4OE	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V <sub>CC</sub>	Positive supply voltage

## FUNCTION TABLE

Inputs		Outputs
nOE	nAx	nYx
L	L	H
L	H	L
H	X	Z

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 Z = High Impedance "off" state

## 3.3V 16-bit inverting buffer/driver (3-State)

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**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +7.0	V
I <sub>OUT</sub>	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V <sub>CC</sub>	DC supply voltage	2.7	3.6	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0		V
V <sub>IL</sub>	Input voltage		0.8	V
I <sub>OH</sub>	High-level output current		-32	mA
I <sub>OL</sub>	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10	ns/V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	°C

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 2.7V; I <sub>IK</sub> = -18mA		-0.85	1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 2.7 to 3.6V; I <sub>OH</sub> = -100μA	V <sub>CC</sub> -0.2	V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -8mA	2.4	2.5		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -32mA	2.0	2.3		
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 100μA		0.07	0.2	V
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 24mA		0.03	0.5	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 16mA		0.25	0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 32mA		0.30	0.5	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 64mA		0.40	0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins	0.1	±1.0	μA
		V <sub>CC</sub> = 0 or 3.6V; V <sub>I</sub> = 5.5V		0.4	10	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub>	Data pins <sup>4</sup>	0.1	1	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 0		-0.4	-5	
I <sub>OFF</sub>	Output off current	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5V		0.1	±100	μA
I <sub>HOLD</sub>	Bus Hold current A inputs <sup>6</sup>	V <sub>CC</sub> = 3V; V <sub>I</sub> = 0.8V	75	135		μA
		V <sub>CC</sub> = 3V; V <sub>I</sub> = 2.0V	-75	-135		
		V <sub>CC</sub> = 0V to 3.6V; V <sub>CC</sub> = 3.6V	±500			
I <sub>EX</sub>	Current into an output in the High state when V <sub>O</sub> > V <sub>CC</sub>	V <sub>O</sub> = 5.5V; V <sub>CC</sub> = 3.0V		50	125	μA
I <sub>PU/PD</sub>	Power up/down 3-State output current <sup>3</sup>	V <sub>CC</sub> ≤ 1.2V; V <sub>O</sub> = 0.5V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> OE/OE = Don't care		1	±100	μA
I <sub>OZH</sub>	3-State output High current	V <sub>CC</sub> = 3.6V; V <sub>O</sub> = 3.0V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		0.5	5	μA
I <sub>OZL</sub>	3-State output Low current	V <sub>CC</sub> = 3.6V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		0.5	-5	
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		0.07	0.12	mA
I <sub>CCL</sub>		V <sub>CC</sub> = 3.6V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		4.0	6.0	
I <sub>CCZ</sub>		V <sub>CC</sub> = 3.6V; Outputs Disabled; V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0 <sup>5</sup>		0.07	0.12	
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 3V to 3.6V; One input at V <sub>CC</sub> -0.6V, Other inputs at V <sub>CC</sub> or GND		0.1	0.20	mA

## NOTES:

- All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND
- This parameter is valid for any V<sub>CC</sub> between 0V and 1.2V with a transition time of up to 10msec. From V<sub>CC</sub> = 1.2V to V<sub>CC</sub> = 3.3V ± 0.3V a transition time of 100μsec is permitted. This parameter is valid for T<sub>amb</sub> = 25°C only.
- Unused pins at V<sub>CC</sub> or GND.
- I<sub>CCZ</sub> is measured with outputs pulled to V<sub>CC</sub> or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

## AC CHARACTERISTICS

GND = 0V; t<sub>R</sub> = t<sub>F</sub> = 2.5ns; C<sub>L</sub> = 50pF; R<sub>L</sub> = 500Ω; T<sub>amb</sub> = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V <sub>CC</sub> = 3.3V ± 0.3V			V <sub>CC</sub> = 2.7V	
			MIN	TYP <sup>1</sup>	MAX	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nAx to nYx	1	0.5 0.5	1.8 2.0	3.2 3.2	4.0 4.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to High and Low level	2	1.0 1.0	2.3 2.1	4.0 4.4	5.0 4.8	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from High and Low Level	2	1.0 1.0	3.2 3.0	4.5 4.4	5.0 4.8	ns

## NOTE:

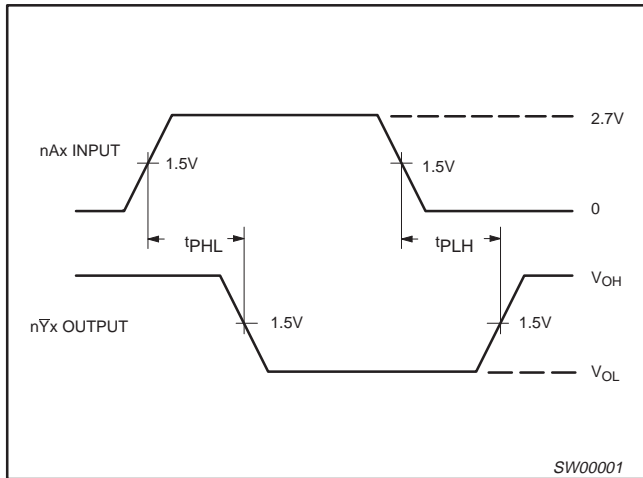
- All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

# 3.3V 16-bit inverting buffer/driver (3-State)

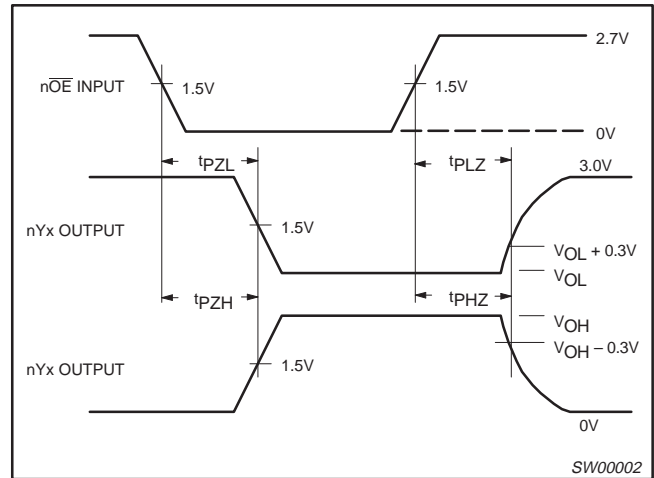
# 74LVT16240A

## AC WAVEFORMS

$V_M = 1.5V$ ,  $V_{IN} = GND$  to  $2.7V$



Waveform 1. Input (nAx) to Output (nYx) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for 3-State Outputs**

**SWITCH POSITION**

TEST	SWITCH
$t_{PHZ}/t_{PZH}$	GND
$t_{PLZ}/t_{PZL}$	6V
$t_{PLH}/t_{PHL}$	open

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

**$V_M = 1.5V$   
Input Pulse Definition**

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_R$	$t_F$
74LVT16	2.7V	$\leq 10MHz$	500ns	$\leq 2.5ns$	$\leq 2.5ns$

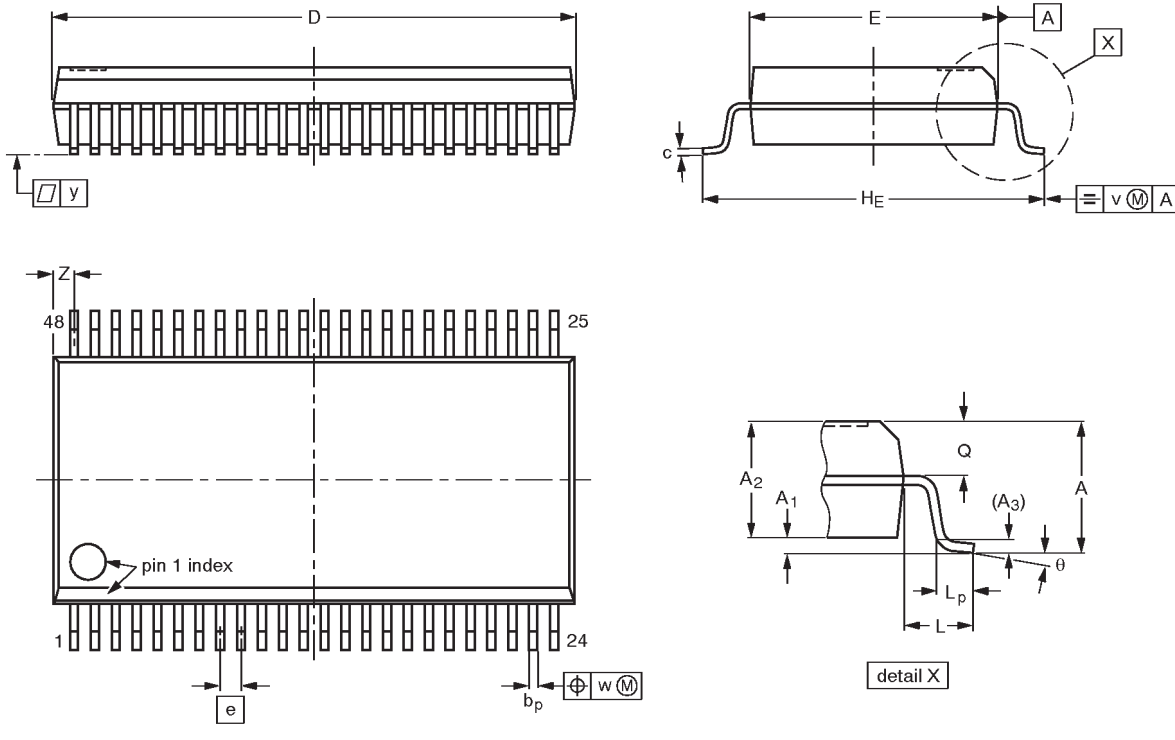
SW00003

# 3.3V LVT 16-bit inverting buffer/driver (3-State)

# 74LVT16240A

**SSOP48:** plastic shrink small outline package; 48 leads; body width 7.5 mm

**SOT370-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

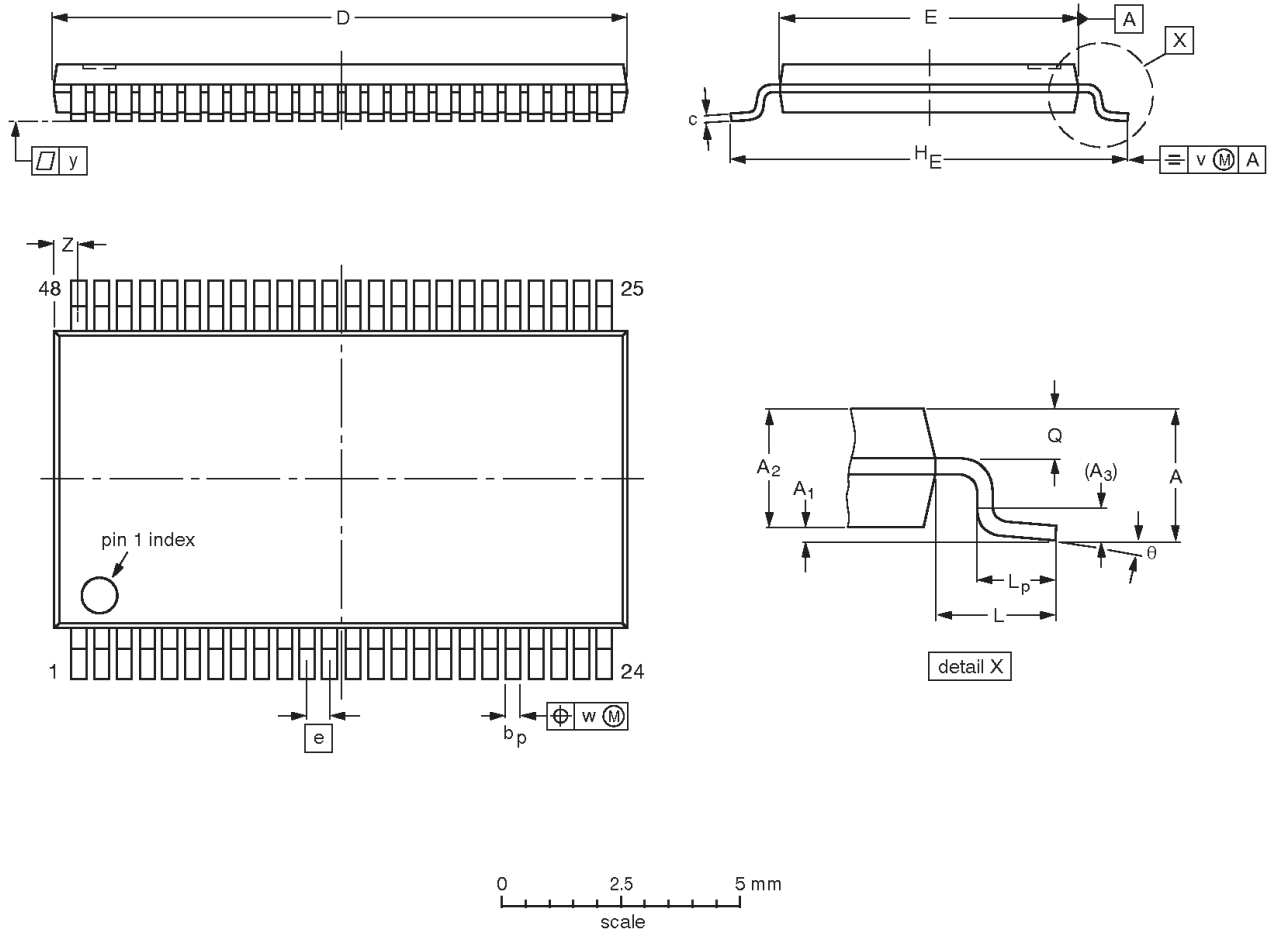
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				93-11-02- 95-02-04

# 3.3V LVT 16-bit inverting buffer/driver (3-State)

# 74LVT16240A

**TSSOP48:** plastic thin shrink small outline package; 48 leads; body width 6.1mm

**SOT362-1**



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153ED				93-02-03 95-02-10



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3.3V LVT 16-bit inverting buffer/driver (3-State)

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**NOTES**

## 3.3V LVT 16-bit inverting buffer/driver (3-State)

74LVT16240A

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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